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EXAMINER	
PORTKA, GARY J	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 9

Application Number: 09/896,157
Filing Date: June 28, 2001
Appellant(s): WILSON ET AL.

Tuan Ngo
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 4, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-12 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,297,265 FRANK et al. 3-1994

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Frank et al., U.S. Patent 5,297,265 (hereinafter "Frank").

As to claims 1-12, Frank discloses the *method, system, and medium for managing memory in a computer system, comprising:*

for at least one memory page, dividing the page into a plurality of relocation blocks ("subpages"), and *placing them at a plurality of locations including one or a plurality of memory systems* (see Abstract: "each with a memory element that stores data pages made up of plural subpages"; col. 11 lines 23-30: "shares data between caches in units of subpages"; and col. 11 lines 52-54: "migrating data and copies of data on a subpage basis from place to place in the system");

using a relocation table having a plurality of entries (cache directories 56x, Fig. 2B and Fig. 5) *to locate the relocation blocks, wherein upon a memory access, using the table to convert an address of a memory page* (SVA = System Virtual Address, Fig. 5) *to a relocation address* (Address Within Cache, Fig. 5) *of a relocation block containing the data intended for the memory access* (see col. 3 lines 39-42; col. 11 lines 59-63: "In data access mode ... satisfy that access by finding the subpage"; col. 12 lines 9-12 and 18-19: Each cache "allocates space for data on a page by page basis" and "stores data on a subpage by subpage basis", and "may or may not contain all of the

page's subpages"; col. 12 lines 20-28: "associations between cache pages and SVA pages are recorded by each cache in its cache directory" and "Each cache directory is made up of descriptors."; col. 12 lines 29-68, which describes how the cache directories find and use descriptors for a particular SVA page; col. 13 lines 1-3: "descriptors contain the following fields"; col. 14 lines 1-4: "Set by cache to record that the corresponding subpage is subcached in the processor on the cache's cell"; and col. 15 lines 52-56: "When a subpage is resident in a cache, the descriptor in that cache for the page containing that subpage records the presence of that subpage"); *and*

if the data intended for the memory access is not in physical memory, then loading in physical memory one or a plurality of relocation blocks containing the data related to the memory access (see col. 16 lines 1-13: states that if a subpage containing requested data in not present in a local cache, it must be acquired "over the domains", which are depicted in Fig. 1; clearly with the recognition of "page fault" at col. 14 line 26, and that modified pages are written to disk at col. 32 lines 57-65, this embodies data "not in physical memory" as recited).

Regarding the dependent claims 2-4, 6-8, and 10-12, the cited sections also show that the virtual address is converted to the extent recited, the relocation blocks are allocated (in the caches) upon receiving the address, and each entry corresponds to a block as recited.

(11) Response to Argument

In response to Appellants' arguments under VIII. 1) Frank fails to teach ... at pages 4-5 of the brief:

Apellants' argument is that Frank does not disclose that the cache directories have any association with subpages, rather with pages. While the Examiner agrees that the cache directories in Frank record a correspondence between the cache pages and the system pages, as described in the rejection above it is clear that they also, via the subpage descriptor, record correspondence to subpages. The argument regarding whether a page has only one subpage is moot since this was not contended by the Examiner, only that as described above any number of subpages of a page (from one to all) may be stored in a particular cache.

In response the Appellants' arguments under VIII. 2) Frank fails to teach ... at pages 6-7 of the brief:

Appellants' argument that the cache directories of Frank are not used to locate the relocation blocks (i.e., subpages in Frank) appears to be based on the previous erroneous argument that these directories are not associated with subpages. As cited in the rejection above and reiterated here: "When a subpage is resident in a cache, the descriptor in that cache for the page containing that subpage records the presence of that subpage", which clearly shows the descriptors within the entries of the directories do indeed locate the subpages. As shown in Fig. 5 of Frank, an SVA (which is a virtual address of a memory page, note "SVA page" citations above in the rejection) is input at the top, and an address within the cache is output at the bottom. The cache directory was used to convert to that cache address, satisfying the limitation for the relocation table as required by claim 1. That cache address further locates the subpages

requested if present, and thus also meets the limitation of a relocation address as in claim 1.

In response to Appellants' arguments under VIII. 3) Franks' subpage ... at pages 7-8 of the brief:

The argument regarding "locations including one or a plurality of memory systems" is moot because the alternative language allows for either limitation to be considered, and thus one memory system reads on "one or a plurality". The argument that in Frank each page is entirely represented and thus a whole page must be loaded is incorrect; as cited above the page must be allocated, but only subpages need be stored, and the subpages may be scattered at various locations. Further, the argument that the invention in contrast requires only loading one or a plurality of location blocks is not supported by the claim language; that is, *only* is not recited and the language "one or a plurality of location blocks" may be interpreted to include all in the page. Notwithstanding, in Frank a subpage may be requested "over the domains" as cited at col. 16. It appears that if other processors allocated space for a page and even if they stored subpages from that page (which are two separate things, a page could be entirely represented in the system by being entirely allocated, and yet none or only some of it's subpages actually stored in the local memories), a first processor could request a subpage without the remainder of the page. Finally, the arguments that the relocation blocks of the invention are distinguished because they may move within a page, or outside the boundaries of a page, and thus are an independent unit from the page, are not supported by the claim language.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Gary J Portka
Primary Examiner
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March 10, 2004

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